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PHASE-ONLY 128x128 SPATIAL LIGHT MODULATOR BASED ON LASLM TECHNOLOGY

Texas Instruments

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13. ABSTRACT (Maximum 200 words)

This contract was for the purpose of building 128x128 pixel spatial light modulator capable of phase-only modulation using TI's unique flexture beam deformable mirror device (DMD) technology. The flexure beam DMD contains mirror elements that move vertically in response to an electrostatic force. The resulting piston-like motion provides broad range analog phase modulation with minimal amplitude modulation. Problems in the CCD addressing prevented the completion and delivery of a fully functioning device.

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I. INTRODUCTION

This final report describes the technical effort to build a 128 × 128 spatial light modulator capable of phase-only modulation using TI's unique flexure beam deformable mirror device (DMD) technology. The flexure beam DMD superstructure architecture contains mirror elements that move vertically in response to an electrostatic force. The resulting piston-like motion provides broad-range analog phase modulation with minimal amplitude modulation. This approach uses a silicon-based, line-addressed analog circuit for addressing circuitry.

II. ADDRESSING CIRCUITRY

A. Approach

The silicon addressing circuitry underlying the DMD superstructure used NMOS and virtual phase CCD elements developed previously at Texas Instruments for use in our cantilever beam, line-addressed spatial light modulator (LASLM). The addressing circuitry is capable of line-at-a-time addressing of the 128 × 128 element array from a single analog input node. The three major components of the addressing circuit are:

1. Two 256-into-64 charge-coupled shift registers/serial-to-parallel converters
2. 128 high-performance analog driver amplifiers
3. A 7 to 128 line digital demultiplexer.

1. Line-Addressed Modulator Architecture

The basic architecture of the existing line-addressed circuitry for area array DMD modulators is shown in Figure 1. This device consists of a 128 × 128 micromirror array that can be addressed by the underlying MOS transistor array. The drains of the address transistors are the vertical lines of Figure 1. The gates of the address transistors are the horizontal lines controlled by the 7-to-128 digital demultiplexer. The device is electronically addressed line by line, with no pauses in the input data stream. Lines of data are fed continuously into the CCD shift register. As soon as a complete line of data has been loaded, it is serial-to-parallel shifted into the drain line amplifier input stage, and amplification of that line begins as the next line of data is clocked in. The pixel driver transistor is built directly under each pixel. After amplification occurs, the decoder selects and turns on the appropriate row gate line, thus turning on all the pixel driver transistors in that row. This

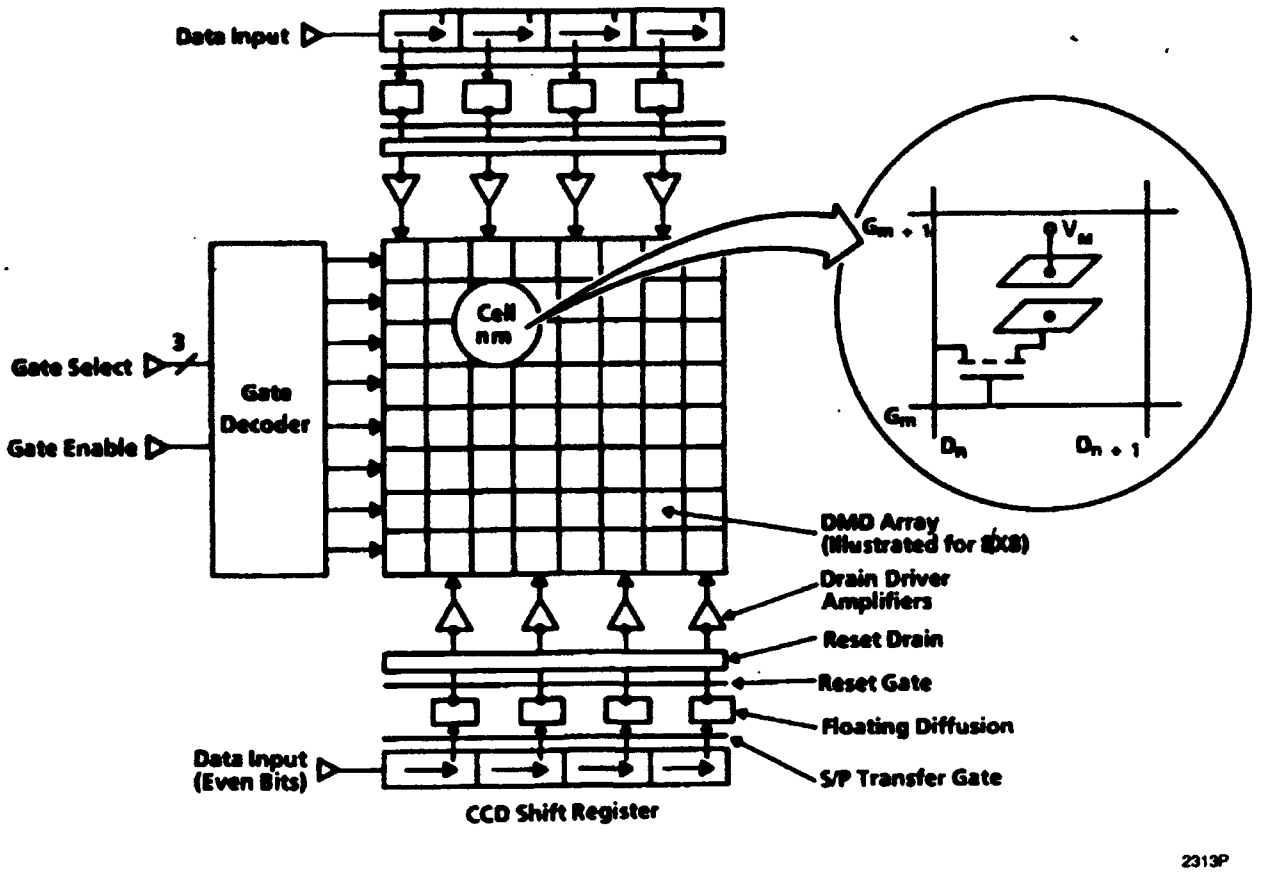


Figure 1.
Functional block diagram of the 128 × 128 line-addressed spatial light modulator.

causes the air gap capacitors (pixels) in that row to charge to the drain voltage levels coming from the drain driver amplifiers. The gate for that row is then turned off, and the capacitors in that row remain charged. Because the other side of the capacitor (the micromirror) is maintained at a fixed bias level V_m, the voltage drop across each air gap capacitor will cause the micromirror to displace toward the silicon surface according to the absolute magnitude of the voltage drain.

B. Results

Testing has been completed on the line-addressed spatial light modulator chips from Lot 8583 (RADC Contract No. F19628-90-C-0134). Unfortunately, the addressing circuitry for the line-addressed chips was not functional. Failure analysis revealed that the yield-limiting components of the addressing circuitry were the CCD serial-to-parallel shift registers and the analog amplifiers. The analog amplifiers were the biggest yield loss. No wafers with working amplifiers were obtained. We suspect that the cause of the low yield on these components of the circuitry was unwanted threshold shifts due to improper ion implant profiles.

C. Addressing Circuitry Background

The addressing circuitry used in the line-addressed architecture was composed of both NMOS and CCD device architectures. The NMOS architecture was used for the column amplifiers while the CCD architecture was used for the serial-to-parallel shift registers. Both of the device architectures (NMOS and virtual phase CCD) used in the line-addressed array are extremely sensitive to the ion implant process. In fact, minor shifts in the implant profile (impurity concentration as a function of depth) can have dramatic effects on the threshold voltages of the devices to the point of rendering the circuit inoperable.

1. CCD Shift Registers

The virtual phase CCD architecture is especially sensitive to minor implant profile shifts since it has one implant (the virtual electrode) that requires the location of the peak to be at the surface of the silicon. If the peak depth is too shallow, the implanted acceptors will be absorbed into the oxide during the anneal. If it is too deep, the boron implant will be fully compensated by previous implants. Either case will result in the surface potential under the virtual electrode being uncontrolled. This will result in CCD shift registers that will not function.

The degree of precision required in the CCD process has historically resulted in low yields. The lot run just prior to this one yielded no working CCDs. To maximize the probability of obtaining working CCDs on this lot, a three-way process split was used on the virtual electrode implant dose. This three way split (three different implant doses were used) at the virtual electrode implant was designed to give us a high probability of getting some wafers within the process window required for proper operation of the CCD. The parameters used in this three way process split were chosen empirically from the test results of the previous lot. (The problem on this previous lot was hypothesized to be caused by the dose of the implant being low.) The lot split was successful, with two of the three implant dose splits yielding functional CCDs. This confirmed the hypothesis that a low dose was responsible for failure of the previous lot, since the lowest dose in the split on this lot also produced nonworking CCDs.

2. NMOS Transistors

The design of the NMOS amplifier was also extremely sensitive to threshold shifts in the transistor channels. The amplifiers were composed of two kinds of transistors—depletion and enhancement mode FETs (these are also known as buried channel and surface channel FETs). The thresholds of the buried channel FETs are controlled using a doubly ionized phosphorus implant that has a deep peak location (this implant also serves as the buried channel for the CCD shift register). Small changes in the implant process can result in a change in the peak location sufficient to have a large impact on amplifier performance. Failure analysis and circuit modeling pointed to this shift in the implant peak location being the cause of the poor amplifier performance.

D. Summary

Both the CCD shift registers and the NMOS amplifiers used ion implant processes that are particularly difficult to control. This resulted in the very poor yield for the line-addressed chips using this architecture.

III. DMD SUPERSTRUCTURE

A. Approach

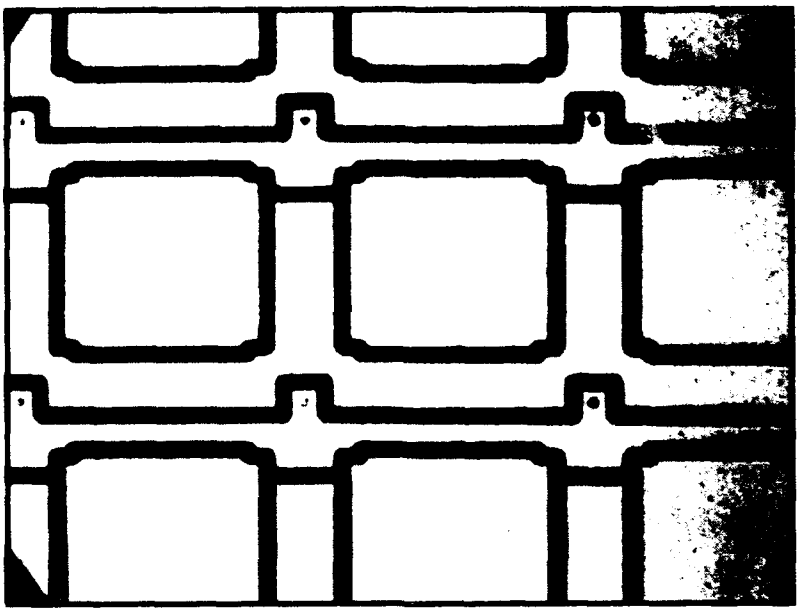
Although the line-addressed circuitry for this lot was not functional, the wafers were used to develop a baseline process for the flexure beam superstructure fabrication. A flexure beam design compatible with the line-addressed architecture was completed and reticles were ordered. The flexure beam pixel size was approximately 50 μm square. A photomicrograph of finished flexure beam devices is reproduced in Figure 2(a) and (b). A schematic cross section is shown in Figure 3.

To maximize the chances of obtaining working flexure beam DMDs from the limited number of wafers in the lot, the DMD superstructure fabrication was completed in phases using two lots. The first lot used process parameters that were our best guess, based on our experience with previous DMD processing and devices, for what would have the highest probability of giving us functional flexure beam devices. The second lot was used to implement changes to the process to increase yield based on the results of the first lot.

The initial process used for the flexure beam device was as close as possible to the standard torsion beam DMD production process used in TI's newly formed manufacturing line (DMD1). This was done to take advantage of the extensive experience and statistical data base available for this process. Where it was deemed necessary for the flexure beam architecture, parameters were varied in a controlled manner from wafer to wafer using process splits. The impact on pixel yield of these splits was then evaluated.

B. First Lot Results

Because the flexure beam pixel architecture (hinge length, beam shape) and mode of operation (noncontact, analog, vertical displacement) are different from the standard torsion beam process (digital rotation about an axis with contact at both extremes), this lot was designed to identify which parameters had the biggest impact on flexure beam yield, uniformity, and electrical performance so that these problems could be addressed in the subsequent lot. Lot splits were incorporated to determine the effect of variations on hinge thickness, hinge length, spacer thickness, and undercut time on pixel yield.



(a) Addressing Electrode Level

(b) Hinge, Post, and Beam Levels

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Figure 2.
Flexure beam DMD design.

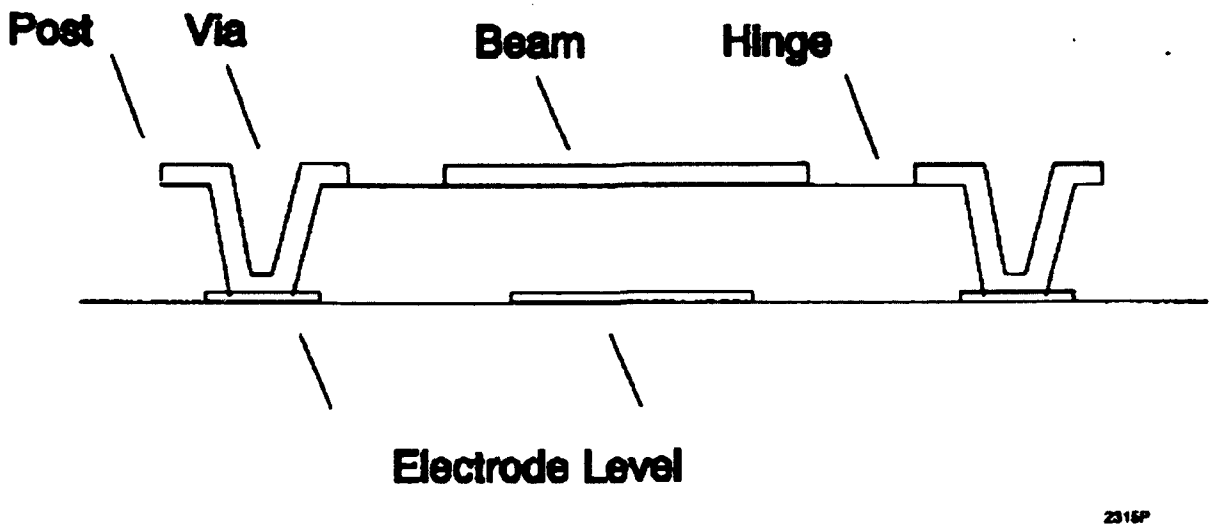


Figure 3.
Flexure beam DMD.

1. Problems

There were several problems that impacted yield in the first lot. The three main problems encountered were hinge compliance, pixel delamination, and pixel webbing. These problems will be described below. Of these three problems, only the hinge compliance problem was specific to the flexure beam architecture.

a. Hinge Compliance

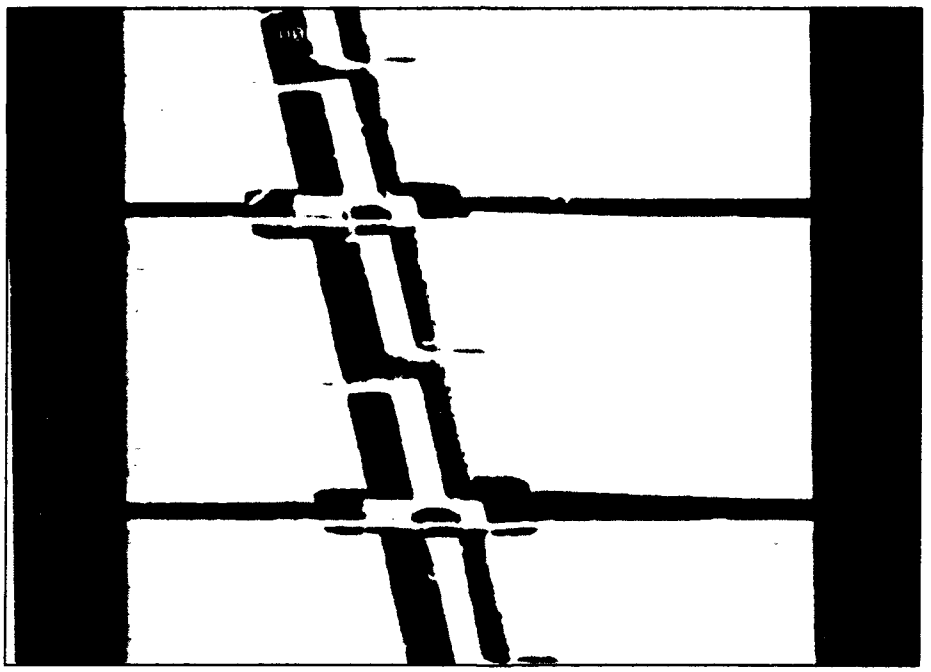
The main problem in Lot 1 was that the hinge metal had insufficient tension to support the flexure beam mirror in the zero bias state. This resulted in virtually all flexure beam pixels being collapsed with no bias applied. This result was somewhat surprising because we intentionally incorporated a hinge thickness split which was designed to give us greater compliance than the standard process (the standard hinge metal thickness of 600 Å was used in this lot as well as a thicker 900 Å deposition). SEM analysis revealed that we did get increased hinge stiffness from the thicker (900 Å) hinge metal (Figure 4). However, this increase in stiffness was still not adequate for proper device operation, and most pixels collapsed after we undercut the resist from the pixels.

b. Other Problems

In addition to hinge compliance, other problems were encountered in the processing of this lot that were not specific to the flexure beam architecture. These included pixel delamination and pixel webbing.

Pixel delamination occurs when the DMD posts do not adhere to the electrodes on the substrate. This can result in the loss of isolated pixels or, if the problem is severe enough, massive

(a) 600 Å Hinge



(b) 900 Å Hinge

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Figure 4.
First flexure beam lot.

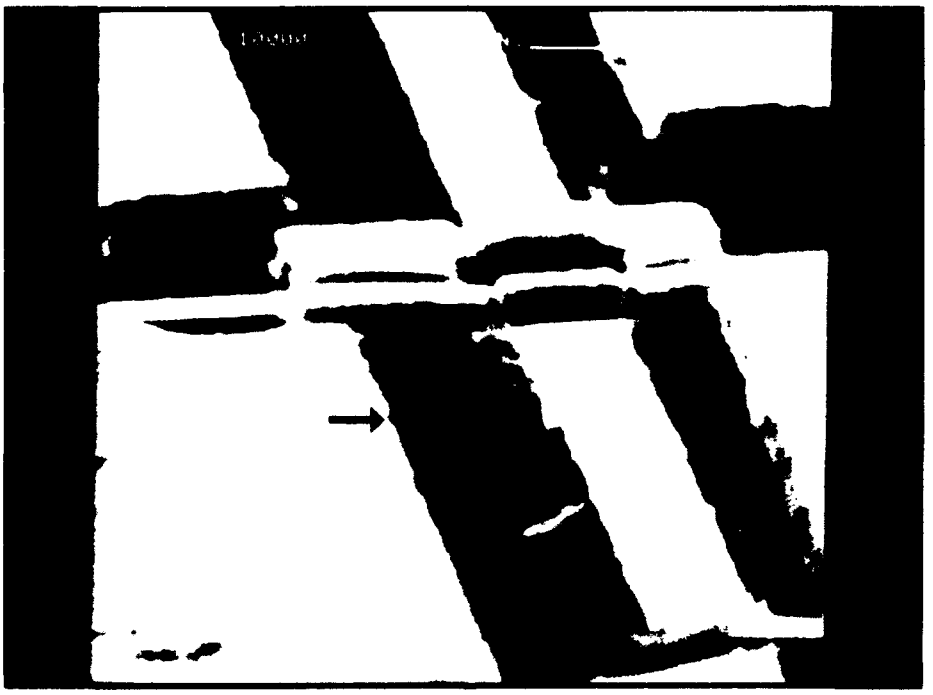
delamination of the entire DMD array. This massive delamination occurred on several wafers in the first lot.

The source of the delamination problem that occurred on Lot 1 was traced to the etching process used to define the vias forming the contact from the DMD mirror surface (called the beam) to the underlying electrode metal (Figure 3). This via etch process sometimes causes the underlying electrode to be partially etched when the via is defined. This etching can cause a depression or trench in the electrode [Figure 5(a)], which, in turn, results in poor step coverage in the beam metal between the via bottom and the via side wall. This trench in the electrode, in combination with the fact that the via etch process gives vias with nearly vertical side walls, results in poor mechanical integrity and as a result, the DMD posts (which are formed from the metal on the side walls of the via) may delaminate from the electrode. Failure analysis using the SEM revealed that the beam metal that goes down into the via and contacts the underlying electrode was indeed discontinuous at the base of the post because of this etching problem [Figure 5(b)]. This resulted in severe post and pixel delamination on several wafers.

One of the main decision points in determining the process flow for Lot 1 was which via process and which spacer stabilization process to use in the DMD process. Although this post delamination problem had occurred intermittently in the past when the via etch process was used (the via is the contact that goes from the beam of the DMD to the electrode on the processor and allows the DMD to be electrically biased), we decided to use the via etch process for several reasons. The main reason this process was chosen is that it is the standard process used in the production of display devices and is therefore fairly routine (although not without problems) and has a large data base associated with it. Another is that it also gives excellent control of the via size and uniformity. An additional reason this process was used was that the alternate process (which is a patterned via followed by a bake process) results in resist flow during bake that broadens the via considerably. We used this patterned/baked process on a previous lot (single quadrant cantilever beam DMD) and found that the vias widen considerably after the resist stabilization bake before DMD metal deposition. Although this has the advantage of giving vias with sloped edges that are good for the beam metal step coverage, it also results in uncontrolled resist flow into the beam region of the DMD. This may cause unwanted and nonuniform tilting of the pixel after undercut, since the hinges follow the contour of the sloped via side wall and connect to the beam at an angle.

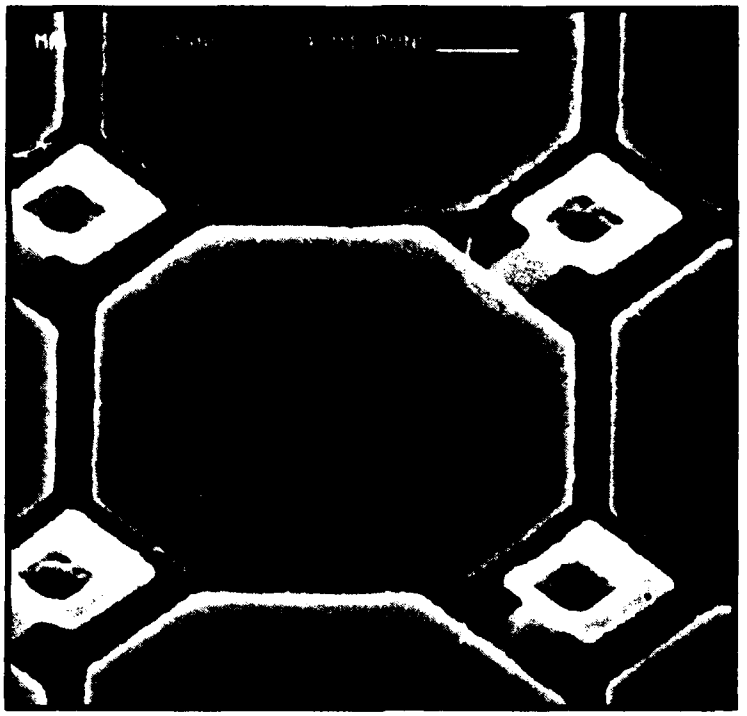
A recent experiment using both of these two via processes in a previous lot (cantilever beam DMDs) using the same addressing circuitry (line-addressed architecture) revealed that the via etch process gave the best overall via size control and uniformity. SEM micrographs from this lot are shown in Figure 6. The vertical side walls and smaller via size on the via etch process are evident in these photos. In spite of its problems, we decided, based on this recent experience, that the overall

(a) Trench in Electrode Level

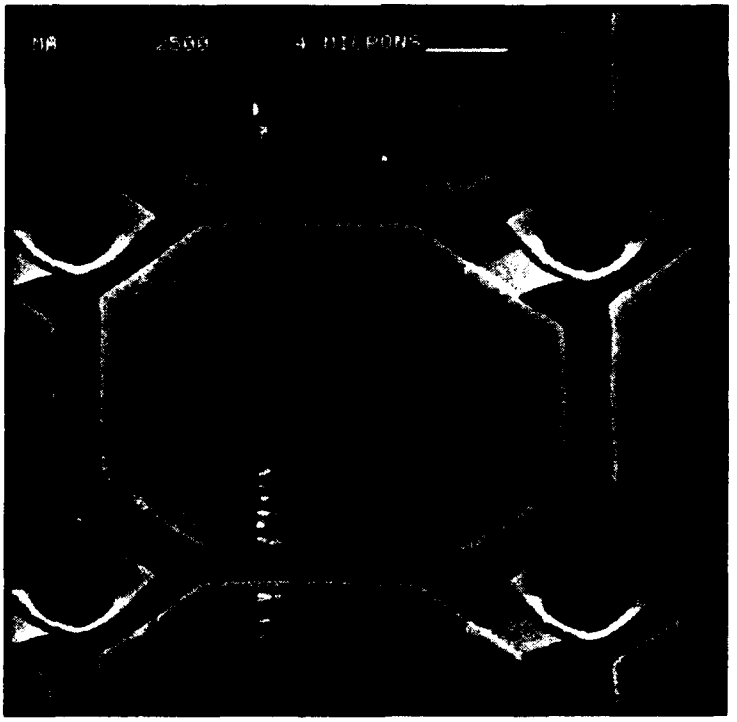


(b) Flexure Beam Post and Hinge (Note Thin Metal at Post Bottom)

Figure 5.
Flexure beam post delamination.



(a) Etched Via Process



(b) Convection Oven-Baked Via Process

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Figure 6.
Single quadrant cantilever beam DMD.

uniformity requirements of the flexure beam architecture would have a better chance of being met with the via etch process. Metal step coverage problems are an intermittent problem and a risk area with this process; however, the via flow problem associated with the alternate process results in known problems that would severely affect performance.

A third problem encountered on Lot 1 was pixel webbing. This manifests itself when all the DMD pixels are held (webbed) together by a thin continuous film after the photoresist is undercut from the pixels. This thin film prevents the pixels from moving freely (Figure 7). This webbing problem was a major yield-limiting factor on all DMD processes (including the standard torsion beam) until a cleanup process was recently introduced to eliminate it. The source of the webbing has been traced to contaminants introduced into the top of the spacer film during beam metal etching (the last major step before undercutting). An acid cleanup was added to the standard production process to eliminate this contaminated top surface without damaging the mirror metal. This allows the mirrors to move freely once the spacer resist is removed from under the mirrors.

This cleanup process was a fairly new addition to the process. It has been found to be necessary on several different device architectures, including the standard torsion beam architecture. On a previous lot using line-addressed architecture, a lot split was used to determine the effect of this cleanup on mirror performance. The cleanup effect was dramatic. Wafers that did not have the acid cleanup were heavily webbed, while those that received the cleanup were completely free of the webbing problem (Figure 8). Because the flexure beam architecture uses the same addressing circuit and the same basic flow as the flexure beam device, we decided, based on these results, to implement this process on the flexure beam flow.

The results of Lot 1 reveal that we had a webbing problem even though the cleanup process was used. After some investigating, we discovered that the source of the webbing problem on this lot was an inadequate cleanup process before DMD undercut (the process in which the photoresist is removed from under the mirrors). This process was not working properly because of a machine malfunction that caused dilution of the etchant responsible for eliminating the unwanted film. This resulted in an incomplete cleanup and pixels that were webbed together.

We determined that both of these latter problems (post delamination and pixel webbing) were due to problems in the process lab that were affecting all lots being run at the time (even the standard torsion beam process). They were not problems having to do with the nonstandard nature of the flexure beam architecture. Both of these problems were addressed by CRL and DMD personnel and changes were implemented to eliminate them.

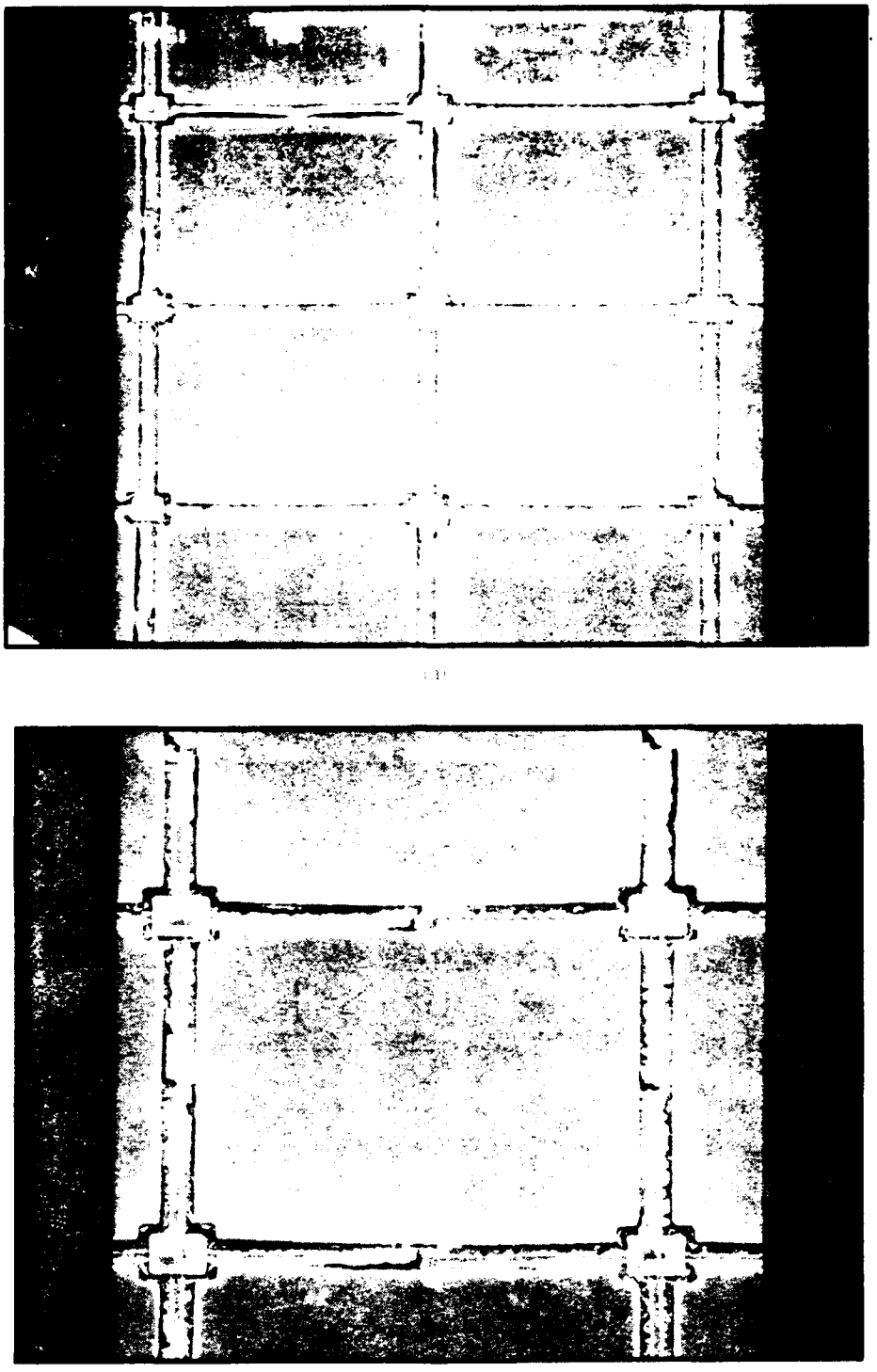
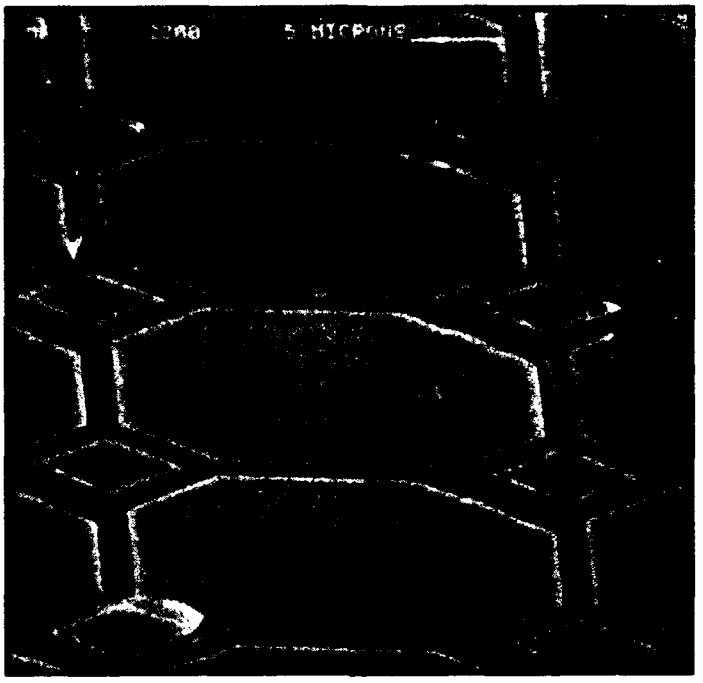
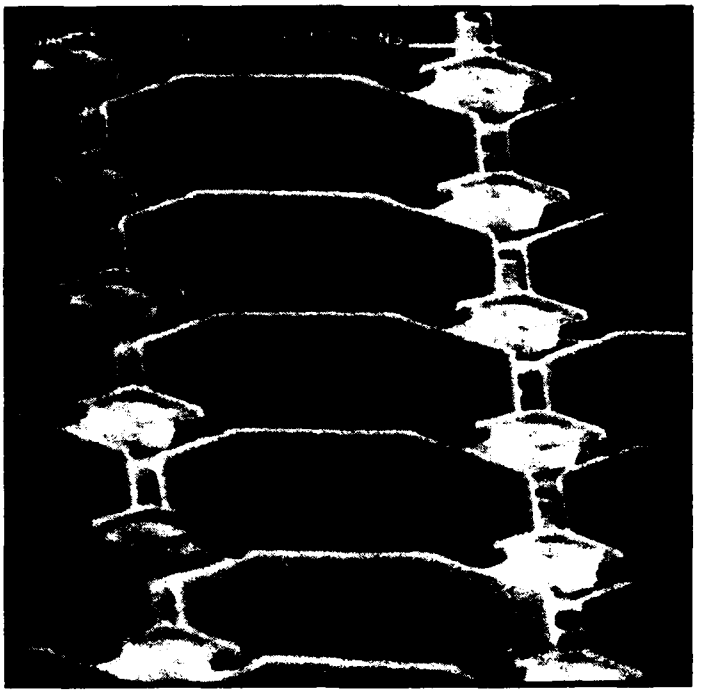


Figure 7.
Flexure beam pixel webbing on Lot 1.



(a) Without Cleanup Process



(b) With Cleanup Process

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Figure 8.
Webbing elimination process.

2. *Favorable Results*

In addition to these problems, several other pieces of information were gathered from the first lot. Extensive undercutting experiments were conducted on all wafers from Lot 1. Inspection of the mirrors after undercut revealed that the thickest spacer (2.5 μm) provided the best yield. The optimum undercut time and process were developed for this spacer thickness (the process seemed relatively immune to variations in the undercut time). These parameters were successfully and efficiently implemented in the second lot.

C. Second Lot Results

Once the problems from the first flexure beam lot were identified, a second lot was started that had processes and wafer splits designed to overcome these problems. The remaining line-addressed wafers were used in this process. The pixel collapse (hinge compliance) problem was addressed by increasing the hinge thickness from 900 Å to 1,200 Å. To address the post delamination problem, process improvements were made in the via etch process to minimize any etching of the electrode. The pixel webbing problem was addressed by fixing the machine malfunction that caused the webbed pixels on the first lot and by requalifying the process on pilot wafers to verify it was, indeed, fixed. As a result of these corrective measures on the second lot, our mechanical integrity and yield improved dramatically. In addition to improved hinge compliance, the webbing and delamination problems that affected Lot 1 were completely eliminated.

Because the pixel delamination and webbing problems were not a factor on the second lot, the dramatic effect on the hinge compliance and pixel yield of increasing the hinge thickness to 1,200Å was readily observable. Although there were still some pixels that collapsed, the pixel collapse problem caused by insufficient hinge tension was greatly reduced.

We gained information regarding pixel yield from test structures on the periphery of the chip in addition to the array area. The test structures were designed to give us information regarding yield variations due to pixel design. The test structures were located on the periphery of each chip and were made up of two types of pixels. One type of test structure had pixels with hinges that were about half the dimension of the beam dimension, and some which had hinges that were a quarter of the beam. We also had two different-sized pixels—25 μm squares and 50 μm squares. Varying the pixel design within the chip allowed us to observe the effect of these variations. This was a useful technique for isolating design-induced effects from processing-related effects on pixel yield because the test structures are on the same chip and, therefore, saw the same process conditions. Using this approach, variations in yield were traced directly to the pixel design.

The test structures revealed that, in addition to the hinge thickness, the hinge length and pixel size were major parameters affecting pixel yield. The test structure pixels with the longer hinges

were less stable (had a greater zero bias deflection) than the shorter hinge pixels. The shorter hinges also tended to result in a more uniform array with respect to pixel tilt and pixel cupping. The drastic improvement in pixel uniformity between a short hinge test structure with a 600 Å hinge (the original process from Lot 1) and a short hinge test structure with 1,200 Å hinge (the best process from Lot 2) is very evident under an interferometric microscope (Figure 9).

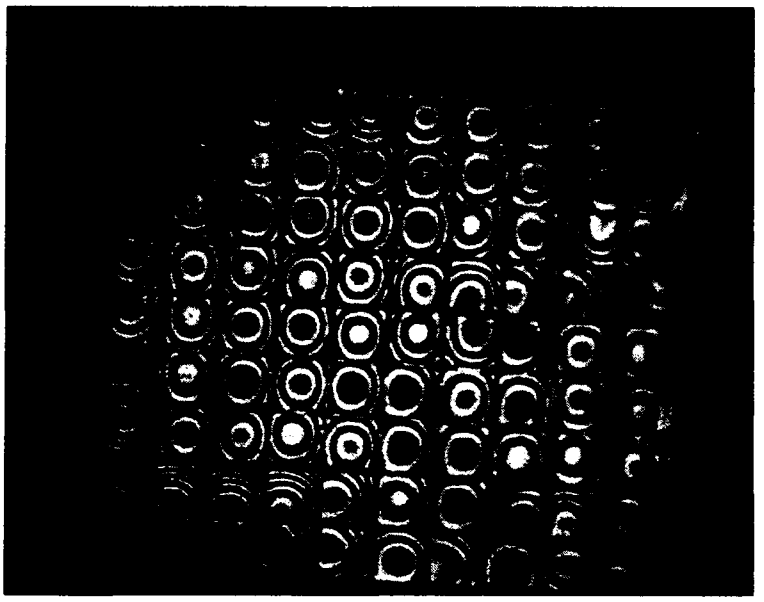
Because the test structures were designed to give us information independent of the addressing circuit functionality, we were able to electrostatically deflect some of the pixels in the test structures on the periphery of the chip. Test structure devices consisted of 10×10 arrays of flexure beam pixels of various sizes on the periphery of the chip. Because the pixels in these arrays were all biased simultaneously and were not individually addressable, one shorted pixel in the array of 100 pixels could cause the entire array to be nonfunctional. This made the yield on test structures very low. However, after carefully developing a robust undercut process and screening many devices, we were able to observe pixel deflection of half a fringe at an 8 V addressing bias on several chips.

D. Flexure Beam DMD Process Summary

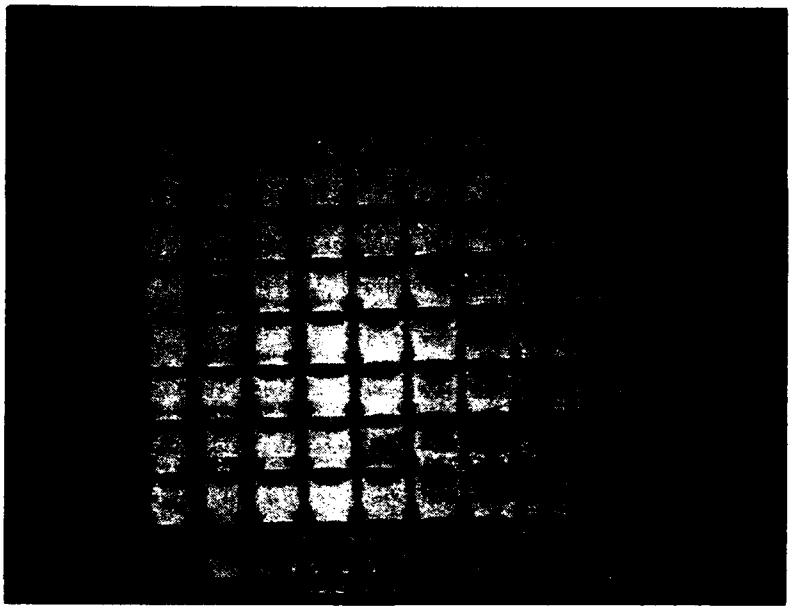
Through this effort, the limits of the standard torsion beam DMD process were determined for the flexure beam device. The standard process proved to be inadequate for the flexure beam DMD. By using two process iterations, we were able to improve substantially the mechanical yield of the flexure beam pixels. This approach allowed us to develop a baseline process for the flexure beam DMD using the nonfunctional line-addressed wafers as an experimental vehicle. We determined empirically that the main variables impacting yield in the flexure beam DMD process were hinge thickness and hinge length. Using this knowledge, the process could be further optimized for pixel cupping and uniformity in the future through more experiments on hinge length and thickness. These further experiments should optimize the process for even greater mechanical integrity, uniformity, yield, and pixel flatness.

ACCOMPLISHMENTS

- We determined limits of baseline torsion beam manufacturing process for flexure beam application.
- We established a baseline process for flexure beam devices with increased mechanical integrity.



(a) Test Structure With 600 Å Hinge



(b) Same Test Structure Type With 1,200 Å Hinge

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Figure 9.
Interferograms showing improved uniformity with thicker hinge metal.

TECHNOLOGY ASSESSMENT

Valuable insight into the flexure beam yield as a function of process parameters was obtained through this effort and should be readily applicable to the next attempt at manufacturing flexure beam DMD arrays.

Unfortunately, we were unable to explore fully the potential of the phase-only flexure beam DMD modulator in this effort because of limitations in the addressing circuitry yield. The next iteration in the development process will use a CMOS addressing circuit manufactured using a mature, well-characterized process that is more in line with TI's current product line. This will give us a high-yield, high-performance processor that will allow us to explore fully the potential of the flexure beam DMD for optical processing applications. A fully functional analog processor in combination with the flexure beam device developed in this effort looks very promising for phase-only spatial light modulators.

MISSION

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